**What is claimed is:**

1. A method for forming a bit line of a semiconductor device, comprising the steps:

(a) forming a P+ S/D region and an N+ S/D region on a semiconductor substrate;

(b) forming a planarized interlayer insulating film on the entire surface of the resulting structure;

(c) etching the interlayer insulating film to form a first opening exposing the P+ S/D region;

(d) subjecting the entire surface of the resulting structure including the first opening to a P+ ion implantation process;

(e) etching the interlayer insulating film to form a second opening exposing the N+ S/D region;

(f) forming a barrier metal layer on the entire surface of the resulting structure including the first and second openings;

(g) forming a tungsten layer filling the first and second openings on the entire surface of the resulting structure; and

(h) selectively etching the tungsten layer and the barrier metal layer to form a bit line.

2. The method according to claim 1, wherein the etching process in the step (c) uses at least one gas selected from the group consisting of $CF_4$, $CHF_3$, $O_2$, Ar and CO.

3. The method according to claim 1, wherein the step (c) further comprises over-etching the exposed P+ S/D region.

4. The method according to claim 3, wherein a depth of the P+ S/D region etched by the over-etching process is 20 to 50% of a thickness of the interlayer insulating film.

5. The method according to claim 4, wherein a depth of the P+ S/D region etched by the over-etching process is 30 to 50% of a thickness of the interlayer insulating film.

6. The method according to claim 3, wherein the over-etching process further comprises performing a post etch treatment (PET).

7. The method according to claim 6, wherein the PET is performed using at least one gas selected from the group consisting of $CF_4$, Ar and $O_2$.

8. The method according to claim 6, wherein the PET is an etching process for etching 20 to 150Å of semiconductor substrate in depth.

9. The method according to claim 8, wherein the PET is an etching process for etching 50 to 150Å of semiconductor substrate in depth.

10. The method according to claim 1, wherein the P+ ion implantation process is performed using $BF_2$ gas.

11. The method according to claim 1, wherein the P+ ion implantation process is performed with an energy ranging from 10 to 30KeV.

12. The method according to claim 11, wherein the P+ ion implantation process is performed with an energy ranging from 10 to 25KeV.

13. The method according to claim 1, wherein the P+ ion implantation process is performed with a dose ranging from $1.0\times10^{-15}$ to $5.0\times10^{-15}$atom/cm$^2$.

14. The method according to claim 13, wherein the P+ ion implantation process is performed with a dose ranging from $2.0\times10^{-15}$ to $4.0\times10^{-15}$ atom/cm$^2$.

15. The method according to claim 1, wherein the etching process in the step (e) uses at least one gas selected from the group consisting of $CF_4$, Ar and $O_2$.

16. The method according to claim 1, wherein the step (e) further comprises over-etching the exposed N+ S/D region.

17. The method according to claim 16, wherein a depth of the N+ S/D region etched by the over-etching process is 20 to 50% of a thickness of the interlayer insulating film..

18. The method according to claim 17, wherein a depth of the N+ S/D region etched by the over-etching process is 30 to 50% of a thickness of the interlayer insulating film.